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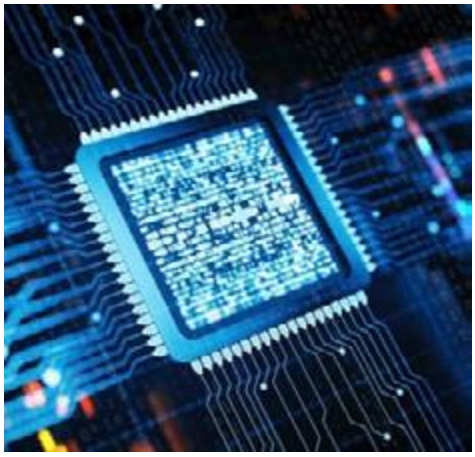
Low Power Latches for Different Precision Needs

Chapman Case #2024-001 and 003



Market Need

In the ever-evolving landscape of graphics processing units (GPUs) and artificial intelligence (AI) systems, power consumption has become a critical concern. The computing power used in AI training has been doubling every 3 to 4 months, driving the need for more energy-efficient solutions. Flip-flops, as one of the main building blocks in a processor's clocking system, can consume more than 50% of the total power. Given the explosive growth in the GPU/AI processor market, which is expected to reach $114.67 billion by 2028, growing at a CAGR of 32.7% from 2021 to 2028, the need for power-efficient flip-flop designs is paramount. This invention's ability to significantly reduce power consumption in a critical component of these high-performance systems could provide a valuable competitive advantage in the marketplace.

Chapman Solution

Dr. Peiyi Zhao of Chapman University has designed a new class of dual-edge-triggering (DET) flip-flop using single-transistor-clocked buffer that completely eliminated both clock and internal redundant transitions, resulting in significantly lower power consumptions compared to the widely used single edge flip flop, TGFF, by 56% at 10% switching activity and 0.8V; It also outperforms existing DET flip-flops, by as much as 14% at 0.4V and 9.5% at 0.8V both at 10% switching activity, respectively.

- The lowest Power-Delay-Product among the state-of-the-art DET designs, improving upon the Floating Node C DET by 53.4% at 0.4V and 51.0% at 0.8V, at 10% switching activity.
- Robust performance across various process corners and Monte-Carlo simulations, demonstrating its reliability and suitability for real-world deployment.
- Scalable design with a low number of clocked transistors (8), which is the least among the state-of-the-art DET flip-flops, further contributing to its power efficiency.
- Versatile topology that can be easily modified to support additional features like scan-chain support and single-edge triggering, providing design flexibility.

This invention also has an iteration that can further reduce power consumptions (~25%) in GPU processors by sacrificing certain level of precision, which is suitable for AI applications such as video/audio processing where perfect calculation is not needed as small inaccuracies can often be tolerated.

Applications

- High-performance computing/gaming
- Cryptocurrency mining
- Data center and cloud computing
- Embedded AI for mobile devices

Key Publication

"Low-Power Redundant-Transition-Free TSPC Dual-Edge-Triggering Flip-Flop Using Single-Transistor-Clocked Buffer", IEEE Transactions on Very Large Scale Integration Systems, May 2023.

Stage of Development

- The proposed flip-flop design has been thoroughly verified through post-layout simulations in a 22nm fully depleted silicon on insulator CMOS technology.
- Patent application filed; available for licensing and further research collaborations.

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